REMARKS

Claims 1-24 are pending in the Application. Claims 1, 9, and 17 are independent. Claim 22 has been amended.

Claim Objections

The Patent Office objected to Claim 22 because the term "poly layer" was unclear. Claim 22 has been amended and is believed clear.

Claim Rejections - 35 USC § 102

The Patent Office rejected Claims 17-18 and 21-23 under 35 U.S.C. § 102(b) as being anticipated by Lee et al. (U.S. Patent No. 6,222,212) ("Lee").

Applicant respectfully traverses the rejection. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983). Emphasis added.

Applicant respectfully submits Claims 17-18 and 21-23 recite elements that have not been disclosed by Lee. For example, Claim 17 generally recites:

> a plurality of platform array units being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one processor;
>
> wherein interconnect between said plurality of platform array units being pre-routed.

The Patent Office cites to Lee for the above limitations (Fig. 7, 700, 721, logic elements, 711, 741-746; and Fig. 9A, circuitry including metal interconnection 913). However, Lee does not disclose a plurality of platform array units being

field programmable wherein interconnect between said plurality of platform array units being pre-routed. A platform array unit is a unit of a field programmable platform array (paragraph 15 of the present application). Lee does not disclose a field programmable platform array. Lee discloses an integrated circuit structure where a base semiconductor structure and a programmable semiconductor structure are fabricated separately so they can be fabricated according to separate design rules and later joined. The integrated circuit structure of Lee is not a unit of a field programmable platform array. An integrated circuit structure where a base semiconductor structure and a programmable semiconductor structure are fabricated separately so they can be fabricated according to separate design rules and later joined is not equivalent to a field programmable platform array.

The Patent Office first compares the field programmable semiconductor device of Lee with the plurality of platform array units of the present invention. A field programmable semiconductor device is merely any semiconductor device which is field programmable. A platform array unit is a unit of a field programmable platform array. Further, the field programmable semiconductor device of Lee is singular, it is not a plurality with pre-routed interconnect. Thus, a field programmable semiconductor device is not equivalent to a plurality of platform array units. The Patent Office then compares the logic elements of Lee with the platform array unit of the present invention. A logic element is merely an electronic device which performs an elementary logic operation. A platform array unit is a unit of a field programmable platform array. Further, the logic elements of Lee are not field programmable. Thus, a logic element is not equivalent to a platform array unit being field programmable. Therefore, Lee does not disclose a plurality of platform array units.

Additionally, Lee does not disclose a plurality of platform array units each of said plurality of platform array units including at least one core and at

least one processor. The Patent Office compares the logic elements of Lee to the at least one processor. A logic element is merely an electronic device which performs an elementary logic operation. A processor is a device which can perform operations on data. A logic element is not equivalent to a processor. Therefore, Lee does not disclose a plurality of platform array units each of said plurality of platform array units including at least one core and at least one processor.

Thus, under *Lindemann*, a *prima facie* case of anticipation has not been established for Claim 17. Claims 18 and 21-23 depend from Claim 17 and are believed allowable due to their dependence upon an allowable base claim.

Claim Rejections - 35 USC § 103

The Patent Office rejected Claims 1-5, 7-13, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over Byrn et al. (United States Patent No. 6,910,201) ("Byrn") in view of Adachi et al. (United States Publication No. 2002/0072135) ("Adachi"). Applicant respectfully traverses.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicant respectfully submits Claims 1-5, 7-13, 15, and 16 recite elements that have not been disclosed by Byrn and Adachi. For example,

Claims 1 and 9 generally recite:

> cutting N by M array of platform array units from a field programmable platform array wafer according to an order from a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one processor, and interconnect between said plurality of platform array units being pre-routed on chip;

The Patent Office cites to Byrn for the above limitations (Fig. 2A, 130; col. 2 lines 1-12; col. 5, lines 30-40; col. 6 lines 20-25; col. 4 lines 36-48; and Fig. 2B, chip, logic element, 132). However, Byrn does not disclose cutting N by M array of platform array units from a field programmable platform array wafer according to an order from a customer, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units.

Byrn does not disclose a field programmable platform array wafer or an array of platform array units. A field programmable platform array wafer is a wafer with all silicon layers and metal layers already built and includes a plurality of platform array units. A platform array unit is a unit of a field programmable platform array (paragraph 15 of the present application). In the cited sections, Byrn discloses generation of clocks and resets in silicon platform chips. A platform chip is a partially manufactured very large scale integration standard integrated circuit that includes standard slices that are designed to perform complex, high level functions, but which have not had all their associated interconnect layers completed. A platform chip is not equivalent to a field programmable platform array wafer or a platform array unit. Thus, Byrn does not disclose a field programmable platform array wafer or an array of platform array units.

Further, Byrn does not disclose cutting N by M array of platform array

units from a field programmable platform array wafer. Byrn does not discuss any cutting. In Byrn, it is not disclosed that the platform chip is cut from anything or that anything is cut from the platform chip. Thus, Byrn does not disclose cutting N by M array of platform array units from a field programmable platform array wafer.

Moreover, Byrn does not disclose a field programmable platform array wafer having all silicon layers and metal layers already built. The platform chip of Byrn does not have all silicon and metal layers already built. One or more metal layers are added later to customize the platform chip. Thus, Byrn does not disclose a field programmable platform array wafer having all silicon layers and metal layers already built.

Additionally, Byrn does not disclose cutting N by M array of platform array units from a field programmable platform array wafer <u>according to</u> an order from a customer. The Patent Office stated every chip is ordered by a customer or customers. However, cutting an N by M array of platform array units from a field programmable platform array wafer <u>according to an order</u> from a customer is not equivalent to a chip being ordered by a customer. Further, the platform chip of Byrn is a standardized chip which is customized by a customer by adding metal layers. The platform chip is not made to order. The platform chip of Byrn may be ordered by a customer, but it is not made specifically for a customer. The platform chip is then customized by adding metal layers. Thus, Byrn does not disclose cutting N by M array of platform array units from a field programmable platform array wafer <u>according to</u> an order from a customer.

Therefore, Byrn does not disclose cutting N by M array of platform array units from a field programmable platform array wafer according to an order from a customer, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of

platform array units. Adachi does not cure the defects of Byrn. For at least these reasons, Claims 1 and 9 are allowable. Claims 2-3, 5, 10, 13-14, 16, 21, 22, and 30-32 are believed allowable due to their dependence upon an allowable base claim.

The Patent Office rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Byrn and Adachi in further view of Wall et al. (U.S. Patent No. 6,507,923) ("Wall"). Claim 6 depends from allowable Claims 1 and is thus allowable based on its dependence on an allowable base claim. Claim 14 depends from allowable Claim 9 and is thus allowable based on is dependence on an allowable base claim.

The Patent Office rejected Claims 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Glen et al. (United States Patent No. 6,962,829) ("Glen"). Claims 19 and 20 depend from allowable Claim 17 and are thus allowable based on their dependence on an allowable base claim.

The Patent Office rejected Claim 24 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of White (United States Publication No. 2004/0068330) ("White"). Claim 24 depends from allowable Claim 17 and is thus allowable based on its dependence on an allowable base claim.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,
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